Amendments to the Specification

Applicants respectfully request Page 9, lines 4 to 20 as previously amended on September 21, 2007 to be further amended as follows:

Figure 3 is a diagram illustrating the cycles used to execute a product operation in an implementation of the encryption processor of the present invention having two multipliers and one adder. Consider the product of the operands (a1, a0) and (b1, b0). In the first cycle, the decode unit 30 issues an instruction (Mult R1 a1,b1 a0,b0). With this instruction, the (a1, b1) and (a0, b0) are simultaneously multiplied using multipliers 36a and 36b respectively. The results of the instruction are then stored in a Register R1. In the second cycle, the decode unit 30 issues another multiplication-add-carry instruction MAC R2 (a1, b0), R1. With this instruction, a1 and b0 are multiplied and the product is added to the contents of R1 and stored in R2. In the third cycle, the decode unit 30 issues another multiply-add-carry instruction MAC R3, (b1, a0) R2. With this instruction, b1 and a0 are multiplied and the product is added to the content of R2 and the result is stored in R3. The product operation is thus executed in three cycles. If this operation was executed in a typical processor, it would have likely required many more clock cycles. For example, the multiplications (a0, b0), (a1, b0), (a0, b1), and (a1, b1) would likely be performed sequentially followed by a series of additions of the intermediate multiplication results to complete the execution of this operation.